Implementing Multipliers in FLEX 10K EABs

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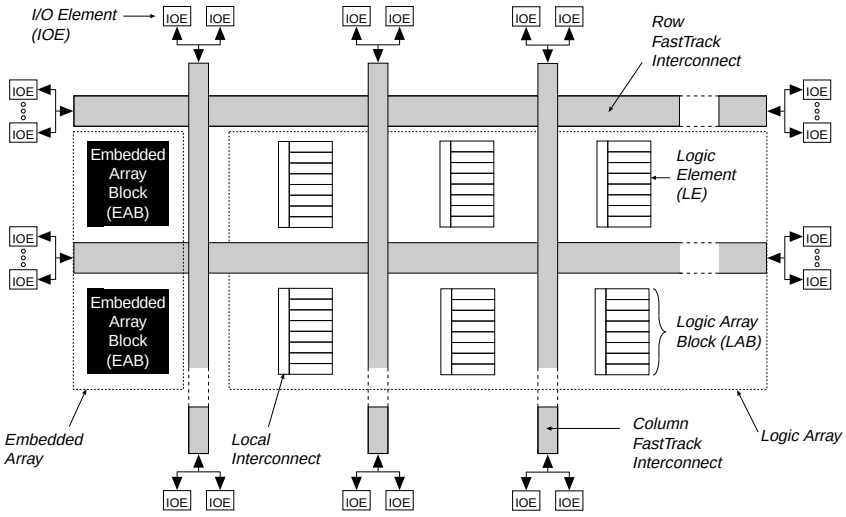
Designers can use the FLEX 10K embedded array for specialized logic functions as well as high-performance, on-chip memory functions. Complex functions implemented in embedded array blocks (EABs) consume fewer device resources and operate faster than functions implemented in logic cells. Because FPGAs are based on logic cells only, FPGA designers must bit-slice and partition complex or high fan-in functions into multiple logic cells. Consequently, the implementation of certain logic functions in an FPGA consumes excessive silicon resources and can incur multiple levels of delays, affecting overall system performance. In contrast, the FLEX 10K architecture, with its embedded array and logic array, improves the performance and efficiency of complex logic functions such as multipliers.

The FLEX 10K Architecture



EABs Allow Elegant Multiplier Implementation

Multipliers, one of the most common functions in digital designs, benefit dramatically from an architecture that contains both an embedded and a logic array. The following example shows the efficiency and performance advantages of the Altera FLEX 10K architecture (EPF10K50-4) relative to the Xilinx XC4000E FPGA architecture (XC4025E-3).

Multiplier Implementation in EPF10K50-4 vs. XC4025E-3

Function	XC4000E Architecture (XC4025E-3)	FLEX !0K Architecture (EPF10K50-4)
4 x 4 Multiplier		
Normalized Die Area	1.0	0.57
Resources Used	18.5 CLBs	1 EAB
Speed	40.3 MHz	73 MHz

The data above was compiled by Altera Applications.

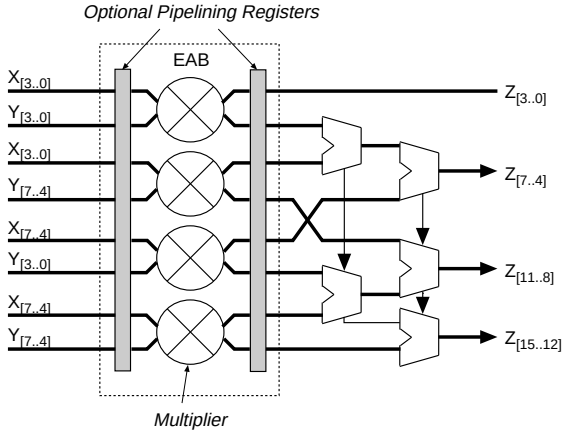
Each EAB can implement a 4 x 4, 5 x 3, or 6 x 2 multiplier. Multipliers with wider inputs or outputs can be split into multiple EABs and still achieve higher performance and efficiency than those implemented only in logic cells.

Self-Contained EAB: Ideal for Pipelined Design

Implementing complex combinatorial functions, such as multipliers, in programmable logic devices typically results in long signal propagation delays. These delays slow down the overall clock speed of a synchronous system. Pipelining is a technique for maintaining high system speed by inserting registers in combinatorial logic paths to keep the paths short. Once the data fills the pipeline, the pipelined design has a higher overall throughput than a design with a long and continuous combinatorial path.

FLEX 10K devices have input and output registers within the EABs, making them ideal for pipelining. Pipelining can increase the system clock rate from 23 to 32 MHz for an 8 x 8 multiplier.

Input and Output Registers of EABs Used as Pipelining Registers



Computation-intensive applications such as digital filtering, data compression, and image processing benefit greatly from high-performance, efficient multipliers. With both an embedded array and a logic array, a FLEX 10K device can implement compact multipliers with higher performance than existing FPGAs.

The documents listed below provide more detailed information. Part numbers are in parentheses.

Product Information Bulletins

PIB 20 *Benefits of Embedded RAM in FLEX 10K Devices (A-PIB-020-01)*
PIB 21 *Implementing Logic with Embedded Arrays in FLEX 10K Devices (A-PIB-021-01)*

Application Notes

AN 53 *Implementing Multipliers in FLEX 10K Devices (A-AN-053-01)*
AN 52 *RAM Functions in FLEX 10K Devices (A-AN-052-01)*

You can request these documents from:

- Altera Express fax service at (800) 5-ALTERA
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